AMENDMENTS TO THE SPECIFICATION:

Please replace paragraphs [13]–[14] with the following amended paragraphs:

[13] Another object of the present invention is to provide an apparatus and method for controlling CPU speed transition, which terminates an SMI service without performing a control operation needed for CPU speed transition when a bus master device is in an active state, but repeatedly generates an event needed for the CPU speed transition.

[14] Another object of the present invention is to provide an apparatus and method for controlling CPU speed transition, which terminates an SMI service without performing a control operation needed for CPU speed transition when a bus master device is in an active state, but repeatedly generates an event needed for the CPU speed transition, for example, a watchdog timer SMI and an embedded controller SMI, at regular time intervals to result in normal CPU speed transition.